REMARKS

Claims 1-5, and 7 have been amended. Claims 8-11 have been withdrawn. Accordingly, claims 1-7 and 12-29 are currently pending.

Specification

Applicants have amended the specification to set forth the title of the invention that was kindly suggested by the Examiner in the Office Action.

Drawings

Applicants respectfully request reconsideration of the requirement to label Figs. 12, 13, 14a and 14b with the legend --Prior Art--. As set forth in the brief description of the drawings, Figs. 12 and 13 are illustrative of a structure of the memory system that is the premise of the invention. Further, Figs. 14a and 14b are explanatory charts for illustrating signal wave form characteristics that the memory modules each receive in the memory system that is the premise of the invention. Further, these figures are discussed on page 4 of the specification, first full paragraph under the heading "Summary of the Invention". Accordingly, Applicants do not describe these figures as representing the prior art,

but rather as representing the premise of the invention. Accordingly, withdrawal of the requirement is requested.

35 U.S.C. §112

Claims 26 and 28 have been rejected under 35 U.S.C. §112, second paragraph, however Applicants request reconsideration of the rejection. In particular, the connecting member referred to in claims 26 and 28 is first mentioned in line 1 of claim 25, from which each of these claims depends. Accordingly, the 35 U.S.C. §112, second paragraph rejection should be withdrawn.

35 U.S.C. §§ 102 and 103

Claims 1, 4, 5 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nakase et al., U.S. Patent No. 6,392,897 (Nakase) in view of Koichiro, JP 1-3971. Further, claims 12-16, 19, 21 and 24-29 stand rejected under 35 U.S.C. §102(e) as being clearly anticipated by Nakase. Reconsideration of these rejections is requested for the following reasons.

Of the independent claims, claim 1 is directed to the memory system of the invention having a memory controller and a plurality of memory modules. Similarly, independent claim

12 sets forth the memory system as comprising a board and a control device and first and second memory modules. With respect to independent claim 25, the connecting member is set forth in combination with a first memory module and a second memory module.

Fig. 1 of the present application shows a memory controller or control device 1 and a plurality of memory modules 2, 3, 4 that are connected by way of a plurality of wirings 12, 13 on a circuit board or board 6. The board 6 comprises a socket (a connecting member) 5 having a plurality of socket pins 10 branched from one point, as shown in Fig. 2. The memory controller 1 and each of the memory modules 2-4 are connected in an equal distance through the socket pins of the socket 5. For example, the socket pins are branched from bus wirings on the board 6, as explained in the paragraph bridging pages 15 and 16 of the specification, with reference to embodiment 1 of the invention. Further, in embodiments 2 and 3 of the invention, the memory controller is connected to each of the plurality of memory modules in an equal distance, as shown in Figs. 10 and Fig. 11, in parallel and radial form, respectively.

With respect to claim 25, the claimed connecting number is supported in the specification by socket 5 and is set forth

as having a first mounting part (where memory module 2 is mounted, for example) having a first terminal (where module 2 is electrically connected, for example). A second mounting part (where memory module 3 is mounted, for example) has a second terminal (where memory module 3 is electrically connected, for example). Where board 6 is to be connected supports the recitation of the third terminal in claim 25. In this arrangement, the first wiring member is connected between the first and third terminal, the second wiring member is connected between the second and third terminal and the length of the first wiring member is equal to the second wiring member.

Neither the primary reference of Nakase nor the secondary reference of Koichiro discloses the claimed combination of the invention. In particular, Nakase merely discloses a memory system having memory sockets, however the reference does not disclose the connecting of a plurality of memory modules by way of a plurality of wirings on a circuit board comprising a socket having a plurality of socket pins branched from one point. Further, the reference does not disclose connecting each of the plurality of memory modules in an equal distance, as set forth in claim 1. Also, the reference does not set forth the combination of claim 12 which includes that the

shortest distance of wirings between the first terminal of the control device and the second terminal of the first mounting part is substantially equal to the shortest distance of wirings between the first terminal of the control device and the third terminal of the second mounting part. Claim 25 also differs from Nakase by setting forth that the length of the first wiring member, which is connedcted between the first and third terminals, is equal to the length of the second wiring member, which is connected between the second and third terminals, as part of the claimed combination.

Koichiro does not disclose the deficiencies of the Nakase reference with respect to the memory controller or control device and the connection between the memory controller and the plurality of memory modules in which the memory controller is connected to each of the plurality of memory modules in an equal distance as set forth in claim 1. Rather, Koichiro merely discloses a connector for a SIMM having a contact (2) that branches from one point of the wirings on a mother printing circuit board (5). Each of the memory modules is connected by using the connector for the SIMM as shown in Fig. 3, however the arrangement does not suggest the claimed connection arrangement set forth by Applicants. Therefore, the combination of the Nakase and Koichiro does not render

claims 1, 4, 5, and 7 unpatentable under 35 U.S.C. §103(a). Further, Nakase is insufficient to anticipate independent claims 12 and 25 and therefore claims 12-16, 19, 21 and 24-29 are not anticipated by Nakase et al.

Claims 2, 3, 17, 18 and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Nakase and Koichiro references and further in view of Billman et al., U.S. Patent No. 4,756,694 and Sanwo et al., U.S. Patent No. 5,530,263. Further, claims 6, 20, and 22 are rejected under 35 U.S.C. §103(a) over the Nakase and Koichiro references, and further in view of Leung et al., U.S. Patent No. 5,592,632. Each of these additionally applied references are applied to the dependent claims and Applicants respectfully traverse these rejections at least for the reason that the independent claims from which these claims depend are patentable over the Nakase and Koichiro references for the foregoing reasons. None of Sanwo, Billman or Leung disclose the deficiencies in the Nakase and Koichiro references that are set forth by Applicants.

Specifically, Sanwo is directed to a memory system having memory sockets, however the reference does not disclose or suggest the connection between the memory controller and the plurality of memory modules being connected by way of a

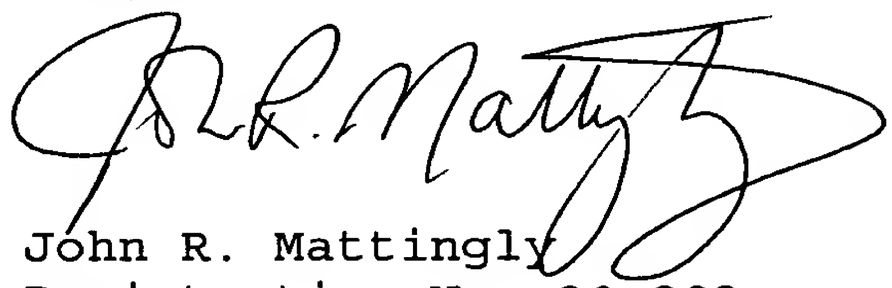
plurality of wirings comprising a socket having a plurality of socket pins branched from one point wherein the memory module is connected to each of the plurality of memory modules in an equal distance.

Billman teaches a plurality of memory modules that are mounted in radial form on a circuit board, however the memory controller is not connected to each of the plurality of memory modules in an equal distance. Further, Leung is merely applied for disclosing the use of a plurality of socket pins of a socket for various signals that are common to each of the plurality of memory modules. However, the reference does not overcome the deficiencies noted with respect to the Nakase and Koichiro references. Therefore, each of claims 2, 3, 6, 17, 18, 20, 22, and 23 are patentable over the art of record and should be allowed with the independent claims from which they depend.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination is requested.

Respectfully submitted,



John R. Mattingly
Registration No. 30,293
Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
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